FIG. 108 is reproduction of FIG. 4f illustrating an array slice to be discussed in connection with the all row high test mode;

FIG. 109 is a reproduction of FIG. 6A with the sense amps and the row decoders illustrated for purposes of explaining the all row high test mode;

FIG. 110 identifies various exemplary dimensions for the chip of the present invention;

FIG. 111 illustrates the bonding connections between the chip and the lead frame;

FIG. 112 illustrates a substrate carrying a plurality of chips constructed according to the teachings of the present invention; and

FIG. 113 illustrates the DRAM of the present invention used in a microprocessor based system.

Microfiche Appendix

Reference is hereby made to an appendix which contains eleven microfiche having a total of sixty-six frames. The appendix contains 44 drawings which illustrate substantially the same information as is shown in FIGs. 1-113, but in a more connected format.